This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A distributed data cache coupled to one of a plurality of heterogeneous processing nodes, wherein the heterogeneous processing nodes are coupled by a programmable interconnection network having a network root and a plurality of crosspoint switches, the distributed data cache ~~as memory or register file~~ comprising:

a first cache memory unit having a plurality of cache ports; and

a plurality of data buses connected with the cache memory unit, wherein each of the plurality of data buses is connected with the plurality of cache ports of the cache memory unit.

2. (Original) The distributed data cache of Claim 1, further comprising a data path adapted for processing data and having at least one data input and at least one data output, wherein the data input and data output are connected with the plurality of data buses.

3. (Original) The distributed data cache of Claim 2, further comprising a multiplexer for alternately connecting the data input with each of the plurality of data buses.

4. (Original) The distributed data cache of Claim 2, further comprising a multiplexer for alternately connecting the data output with each of the plurality of data buses.

1. (Original) The distributed data cache of Claim 1, further comprising a plurality of data address generators connected with a memory unit and the plurality of data buses without latency.

2. (Original) The distributed data cache of Claim 5, wherein the plurality of data address generators are adapted to retrieve a plurality of data values from the memory unit and communicate the plurality of data values to the plurality of data buses directly without any latency due to registering.

3. (Original) The distributed data cache of Claim 6, wherein the plurality of data address generators are adapted to simultaneously communicate the plurality of data values to the plurality of data buses, wherein each of the plurality of data values is communicated to a different one of the plurality of data buses.

4. (Original) The distributed data cache of Claim 7, wherein the first cache memory unit is adapted to simultaneously load a plurality of data values from the plurality of data buses, such that each of the plurality of data values is loaded in a different one of the plurality of cache lines of the first cache memory unit through the same port.

5. (Original) The distributed data cache of Claim 1, wherein the number of cache lines of the first cache memory unit are equal to the number of data buses.

6. (Original) The distributed data cache of Claim 1, further comprising at least one additional cache memory unit also having a plurality of cache lines, wherein each cache line of the additional cache memory unit is connected with the plurality of data buses.

7. (Original) The distributed data cache of Claim 10, wherein the total number of cache memory units is equal to the number of cache lines in each cache memory unit.

8. (Currently Amended) An apparatus for transposing a plurality of data values arranged in a matrix, the apparatus coupled to one of a plurality of heterogeneous processing nodes, wherein the heterogeneous processing nodes are coupled by a programmable interconnection network having a network root and a plurality of crosspoint switches, the apparatus comprising:

a plurality of cache memory units, each cache memory unit having a plurality of cache ports; and

a plurality of data buses, each data bus connected with a different one of the plurality of cache ports from each of the cache memory or register file units.

9. (Original) The apparatus of Claim 12, further comprising a plurality of data address generators adapted to retrieve a plurality of data values from the memory unit and communicate the plurality of data values to the plurality of data buses without any latency.

10. (Original) The apparatus of Claim 13, wherein the plurality of data values comprises a plurality of sets of data values.

11. (Original) The apparatus of Claim 14, wherein the plurality of data address generators are adapted to sequentially communicate the plurality of sets of data values with the plurality of data buses without any register latency.

12. (Original) The apparatus of Claim 15, wherein the plurality of data address generators are adapted to simultaneously communicate the data values of each set of data values to the plurality of data buses without any register latency.

13. (Original) The apparatus of Claim 16, wherein each set of data values is a matrix row.

14. (Original) The apparatus of Claim 16, wherein each set of data values is a matrix column.

15. (Original) The apparatus of Claim 16, wherein each of the cache memory units is adapted to simultaneously load one of the sets of data values from the plurality of data buses, such that each data value of the set of data values is loaded in a different one of the plurality of cache ports of the cache memory unit or register file.

20. (Currently Amended) A method for transposing a plurality of data values arranged in a matrix, the matrix including a plurality of heterogeneous processing nodes coupled by a programmable interconnection network having a network root and a plurality of crosspoint switches, the method comprising:

retrieving a first subset of data values from the plurality of data values from a memory unit;

simultaneously transferring the first subset of data values to a plurality of data buses, wherein each data value of the first subset is transferred to a different one of the plurality of data buses; and

simultaneously loading the first subset of data values from the plurality of data buses to a first cache memory unit having a plurality of cache lines, wherein each cache port receives a data value from a different one of the plurality of data buses without any latency.